What is claimed is:

1. A semiconductor device having an electrically erasable programmable read only memory (EEPROM), comprising

a contactless array of EEPROM memory cells disposed in rows and columns and constructed over a silicon-on-insulator wafer, each EEPROM memory cell comprising a drain region, a source region, a gate region, and a body region;

a plurality of gate lines each connecting the gate regions of a row of EEPROM memory cells;

a plurality of body lines each connecting the body regions of a column of EEPROM memory cells;

a plurality of source lines each connecting the source regions of a column of EEPROM memory cells; and

a plurality of drain lines each connecting the drain regions of a column of EEPROM memory cells;

wherein the source lines and the drain lines are buried lines, and the source regions and the drain regions of a column of EEPROM memory cells are insulated from the source regions and the drain regions of the adjacent columns of EEPROM memory cells.

2. The semiconductor device of claim 1, wherein the EEPROM memory cells include stacked gate structure fabricated on the silicon-on-insulator wafer.

3. The semiconductor device of claim 2, wherein the stacked gate structure includes a control gate region and a floating region separated from the control gate region by an insulating layer.

4. The semiconductor device of claim 3, wherein the floating region is disposed over the body region and is separated from the body region by an insulating layer.

5. The semiconductor device of claim 4, wherein the insulating layer is a silicon oxide film.

6. The semiconductor device of claim 1, wherein the source regions and the drain regions of a column of EEPROM memory cells are insulated from the source regions and the drain regions of the adjacent columns of EEPROM memory cells by one or more oxide layers.

7. The semiconductor device of claim 1, wherein at least one source line of a column of EEPROM memory cells is electrically connected to the body line of the same column of EEPROM memory cells.

8. The semiconductor device of claim 7, wherein the source line and the body line are electrically connected by butting contacts.

9. The semiconductor device of claim 1, wherein the drain region and the source region in one or more of the EEPROM memory cells are disposed in a substantially symmetric structure relative to the gate region and the body region.

10. The semiconductor device of claim 1, wherein the body region comprises a semiconductor material of a first conductivity type, and the source region and the drain region comprise a semiconductor material of a second conductivity type that is opposite to the first conductivity type.

11. The semiconductor device of claim 1, wherein the memory states of the EEPROM memory cells are programmed by applying a first set of one or more voltages at the gate lines and erased by applying a second set of one or more voltages at the gate lines.

12. The semiconductor device of claim 11, wherein the first set of voltages are higher than the second set of voltages.

13. The semiconductor device of claim 12, wherein the first set of voltages are positive and the second set of voltages are negative.

14. The semiconductor device of claim 11, wherein the first set of voltages are lower than the second set of voltages.

15. The semiconductor device of claim 14, wherein the first set of voltages are negative and the second set of voltages are positive.

16. The semiconductor device of claim 11, wherein the EEPROM memory cells are programmed to two or more memory states by applying the first set of two or more voltages at the gate lines.

17. The semiconductor device of claim 16, wherein a row of EEPROM memory cells are programmed to two or more memory states by applying two or more voltages to different

source lines and applying a fixed voltage at the gate line connecting to the row of EEPROM memory cells.

18. The semiconductor device of claim 16, wherein a row of EEPROM memory cells are programmed to two or more memory states by applying two or more voltages to different drain lines and applying a fixed voltage at the gate line connecting to the row of EEPROM memory cells.

19. The semiconductor device of claim 16, wherein a row of EEPROM memory cells are programmed to two or more memory states by applying two or more voltages to different body lines and applying a fixed voltage at the gate line connecting to the row of EEPROM memory cells.

20. A semiconductor device having an electrically erasable programmable read only memory (EEPROM), comprising

a contactless array of EEPROM memory cells disposed in rows and columns and constructed over a silicon-on-insulator wafer, each EEPROM memory cell comprising a drain region, a source region, a gate region, and a body region;

a plurality of gate lines each connecting the gate regions of a row of EEPROM memory cells;

a plurality of source lines each connecting the source regions and the body regions of a column of EEPROM memory cells; and

a plurality of drain lines each connecting the drain regions of a column of EEPROM memory cells;

wherein the source lines and the drain lines are buried lines; and the source regions and the drain regions of a column of EEPROM memory cells are insulated from the source regions and the drain regions of the adjacent columns of EEPROM memory cells.

21. The semiconductor device of claim 20, further comprising at least a plurality of body lines each connecting the body regions of a column of EEPROM memory cells wherein the source line of a column of EEPROM memory cells is electrically connected to the body line of the same column of EEPROM memory cells.

22. The semiconductor device of claim 21, wherein the source line and the body line of a column of EEPROM memory cells are electrically connected by butting contacts.

23. A method for correcting out-of-range threshold voltages of EEPROM memory cells in a semiconductor device, comprising

specifying a tolerance range for the threshold voltage of each memory state for the EEPROM memory cells;

detecting at least one out-of-range threshold voltage in the EEPROM memory cells;

applying a positive voltage pulse to the gate region if the detected out-of-range threshold voltage is below the specified tolerance range; and

applying a negative voltage pulse to the gate region if the detected out-of-range threshold voltage is above the specified tolerance range.

24. The method of claim 23, wherein detecting at least one out-of-range threshold voltage comprises applying a range of voltages to the gate line and sensing the threshold voltages of the EEPROM memory cells.

25. The method of claim 23, further comprising

applying a positive voltage pulse to a gate line if out-of-range threshold voltages are detected below the specified tolerance range at a plurality of EEPROM memory cells connected to the gate line; and

applying a negative voltage pulse to a gate line if out-of-range threshold voltages are detected above the specified tolerance range at a plurality of EEPROM memory cells connected to the gate line.

26. The method of claim 25, further comprising

applying two or more different voltages to different source lines wherein the different voltages correspond to different memory states of the memory cells.

27. The method of claim 25, further comprising

applying two or more different voltages to different drain lines wherein the different voltages correspond to different memory states of the memory cells.

28. The method of claim 25, further comprising

applying two or more different voltages to different body lines wherein the different voltages correspond to different memory states of the memory cells.

29. A method of manufacturing a semiconductor device having an electrically erasable programmable read only memory (EEPROM) having a plurality of EEPROM cells, comprising:

providing a silicon-on-insulator (SOI) wafer comprising a top silicon layer of a first conductivity type;

growing a gate insulation film over the top silicon layer;

depositing a floating-gate layer over the gate insulator;

patterning the floating-gate layer and the gate insulation film in a first photo-masking step to form floating-gate structures in column-wise stripes.

implanting impurities on the top silicon layer to form heavily doped areas of a second conductivity type, wherein the heavily doped areas are self-aligned to the floating-gate structures;

forming insulating floating-gate sidewall spacers on the side walls of the column-wise floating-gate structures;

removing the heavily doped area in the exposed top silicon layer between the insulating floating-gate sidewall spacers by etching to form electrically isolated heavily doped areas and grooves between the electrically isolated heavily doped areas, wherein the grooves and the electrically isolated heavily doped areas are self-aligned to the floating-gate structures;

forming a first insulation film over the grooves between the two heavily doped regions, wherein the first insulation film is in stripe-wise pattern and self-aligned to the floating-gate structure;

forming an inter-gate dielectric layer over the wafer;

depositing a control gate layer over the wafer;

patterning the control gate layer to form row-wise control-gate stripes in a second photo-masking step; and

removing the floating-gate structures not covered by the control-gate stripes by etching such that the remaining floating-gate structures are self-aligned to the control-gate stripes.

30. A method of claim 29, wherein the EEPROM cells comprise source regions and drain regions formed in the electrically isolated heavily doped areas in the top silicon layer.

31. A method of claim 29, further comprising

depositing a first sacrificial insulating film over the floating-gate layer after the floating-gate layer is deposited over the gate insulator;

patterning the first sacrificial insulating film in the first photo-masking step such that the floating-gate structures further include the first sacrificial insulating film; and

removing the sacrificial insulating film before an inter-gate dielectric layer is formed over the wafer.

32. A method of claim 29, further comprising

forming conductive floating-gate sidewall spacers on the side walls of said column-wise floating-gate structures before an inter-gate dielectric layer is formed over the wafer, wherein the floating-gate sidewall spacers are electrically connected with the floating-gate layer and the floating-gate sidewall spacers are self-aligned to the floating-gate structures.